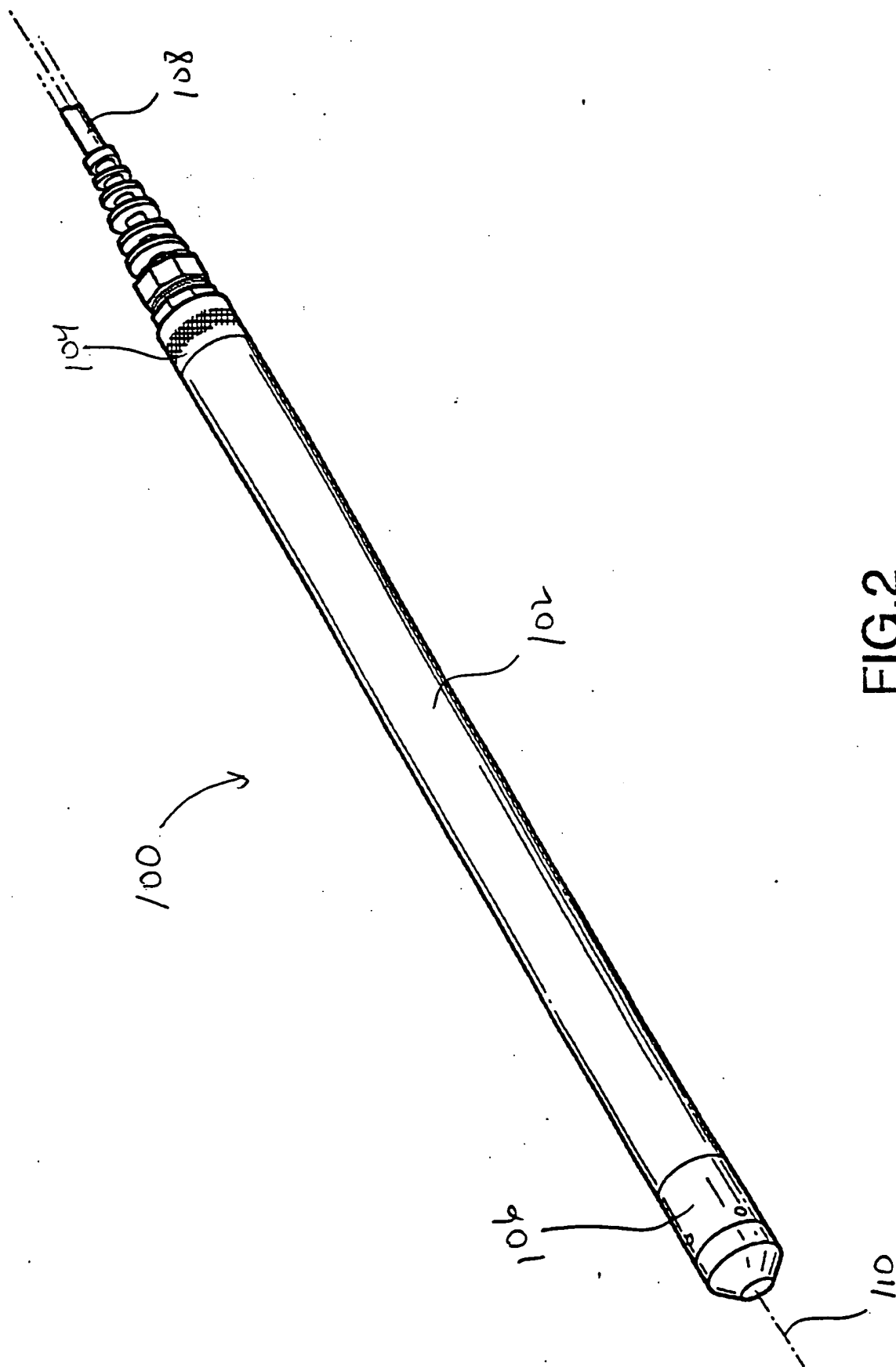


FIG.1

[illegible]

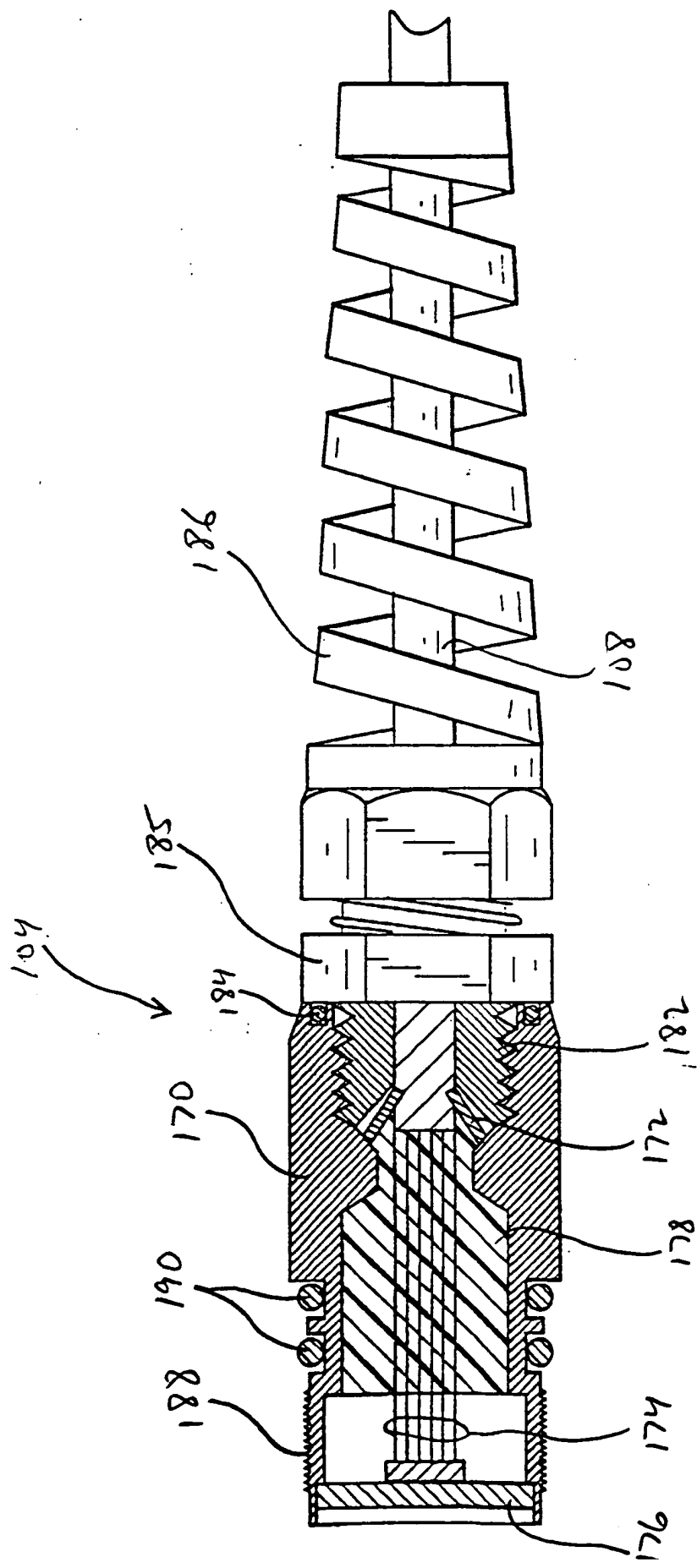


FIG.4

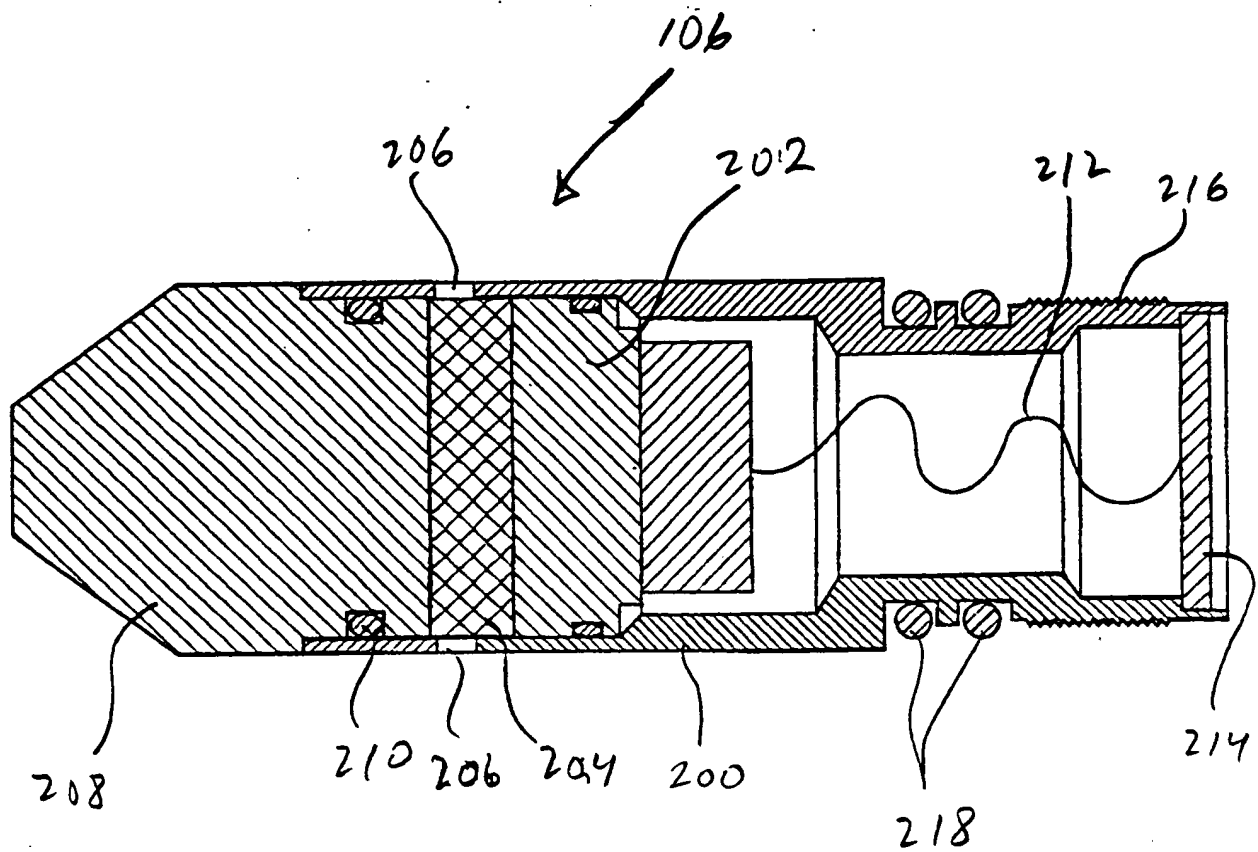


FIG.5

100

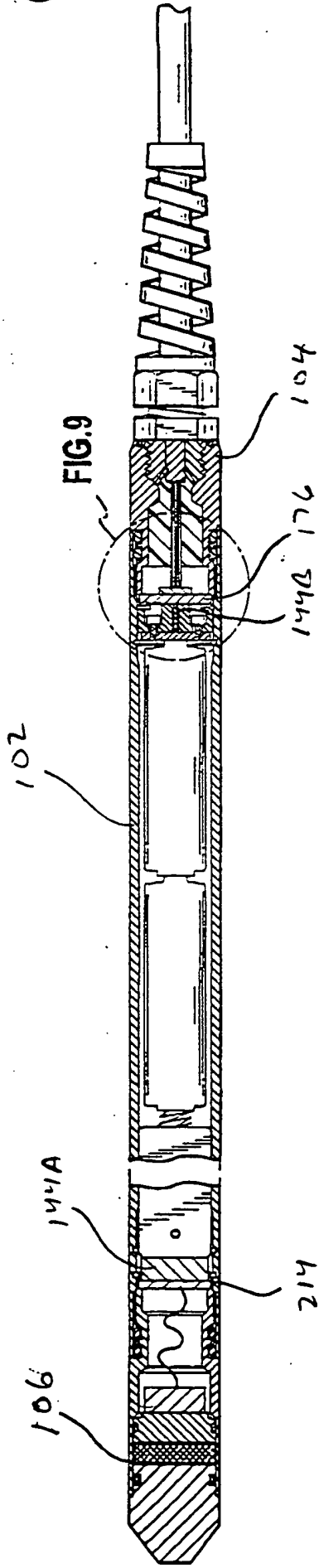


FIG. 6

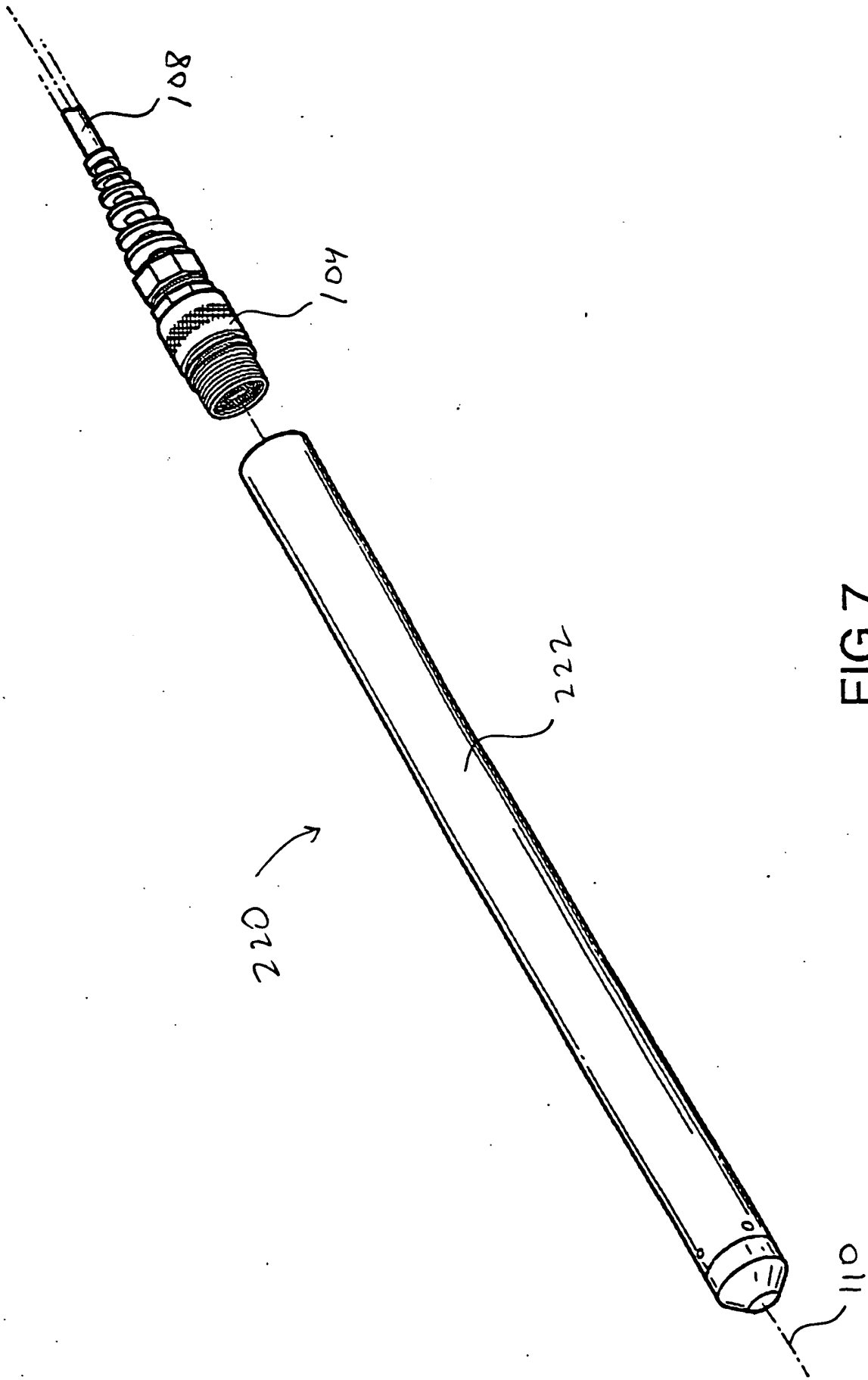


FIG.7

220

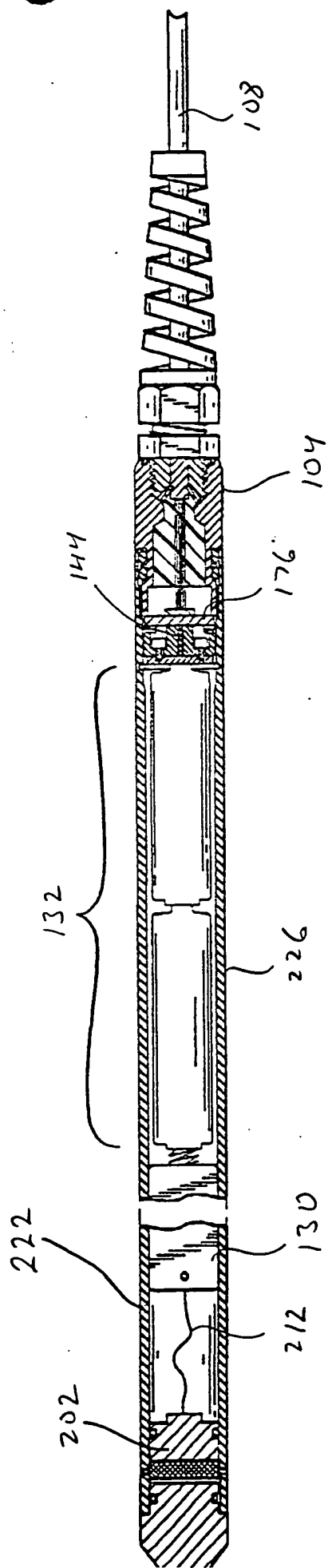


FIG.8

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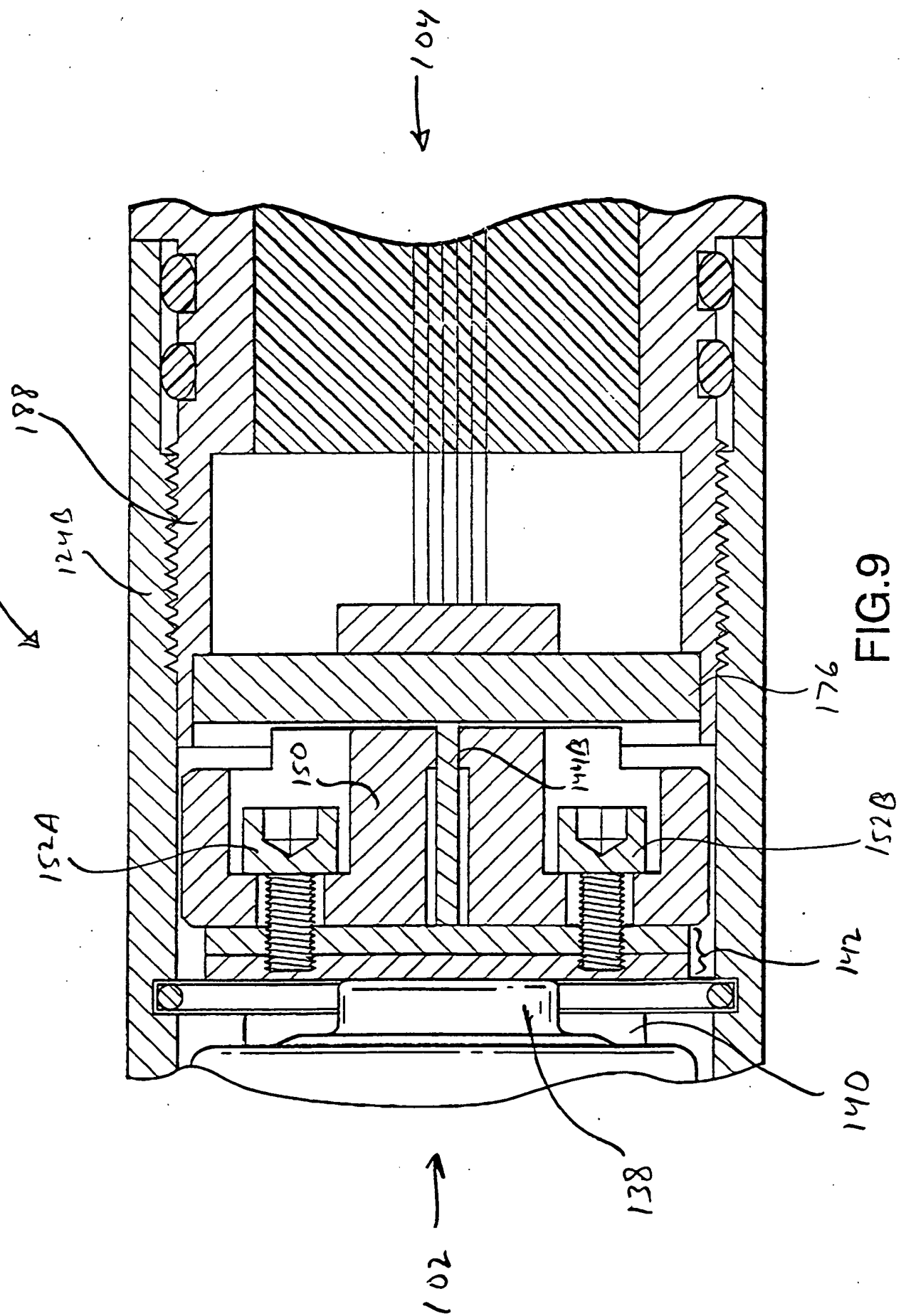


FIG. 9

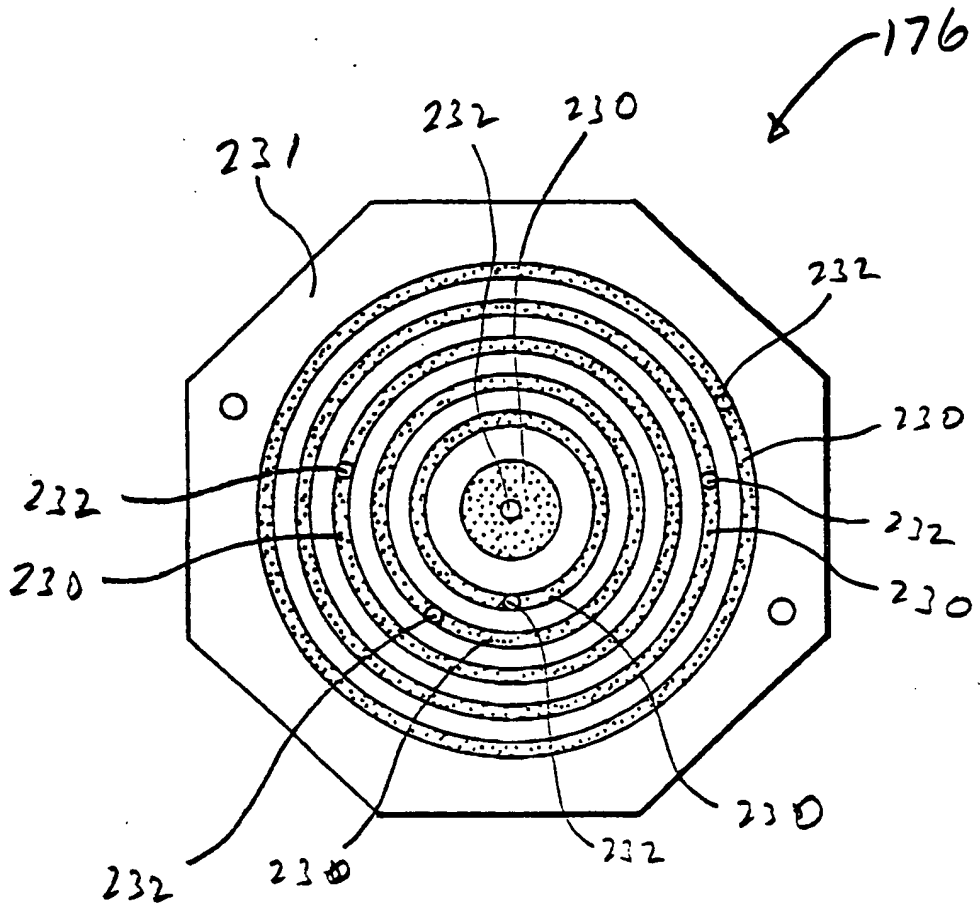


FIG. 10

000000-09922960

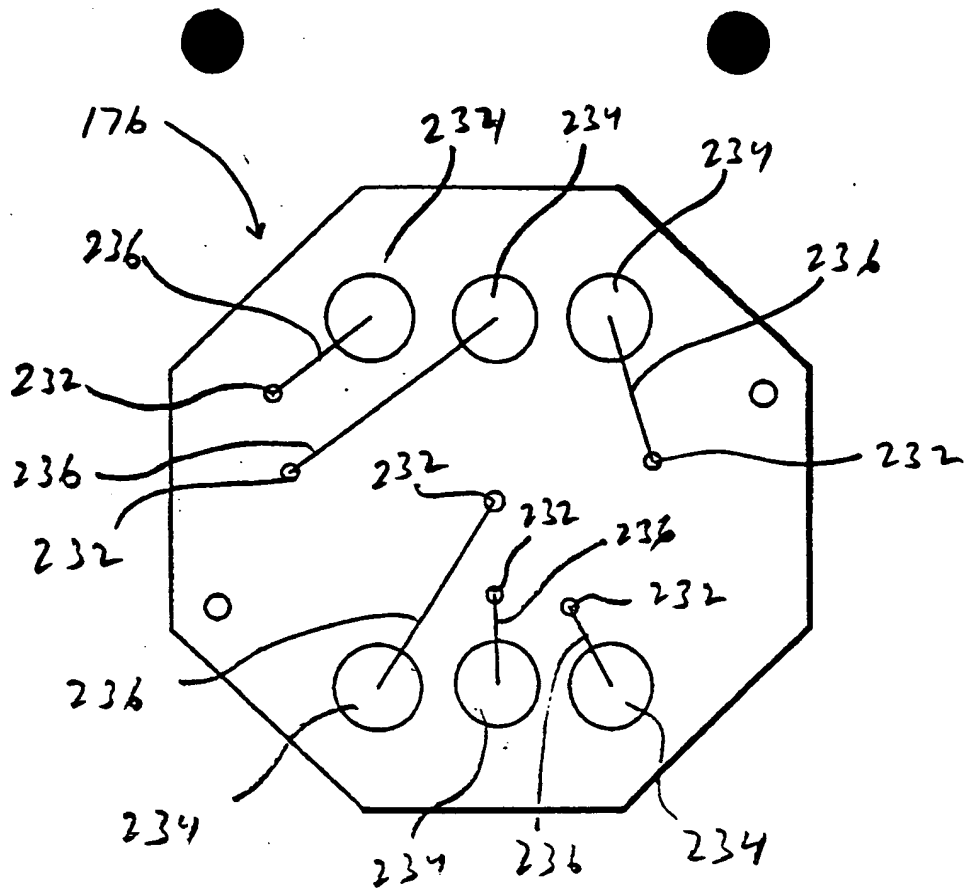


FIG. 11

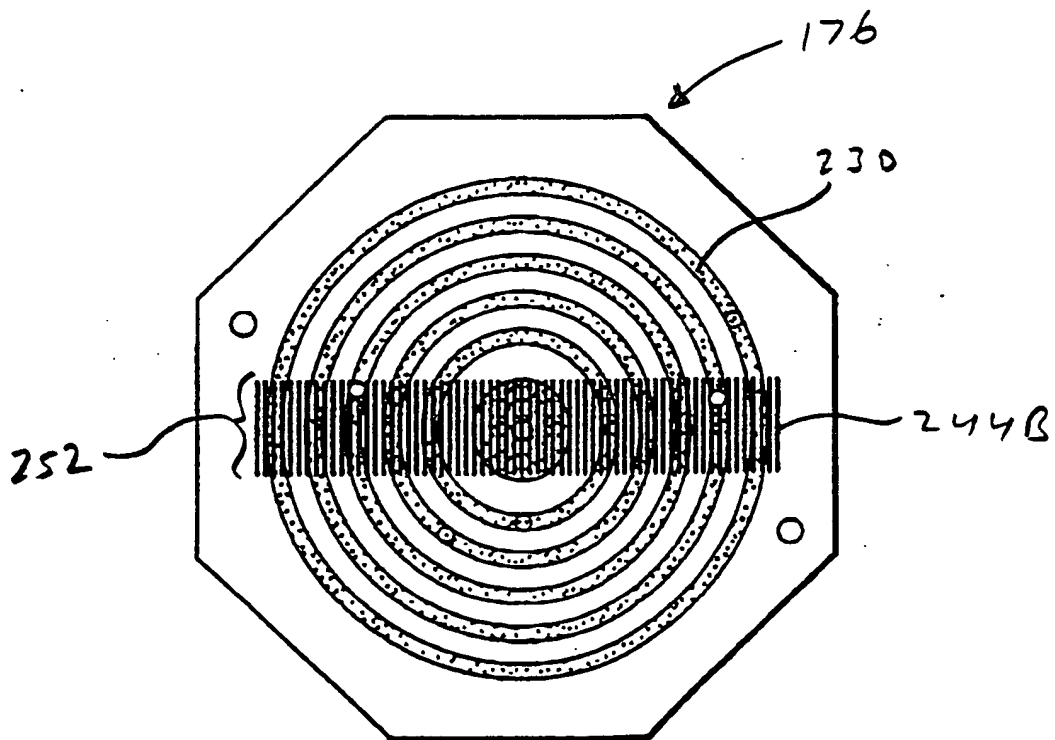


FIG. 14

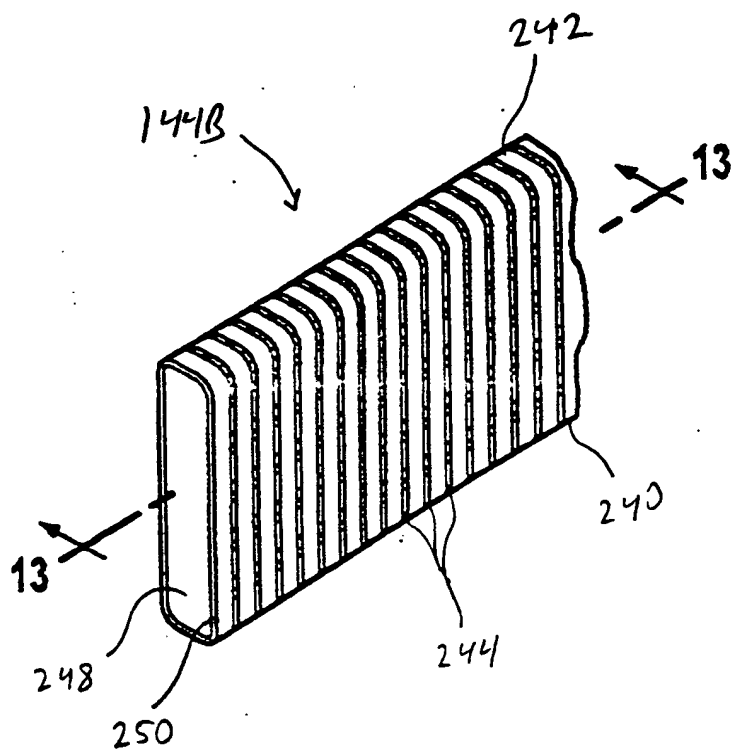


FIG. 12

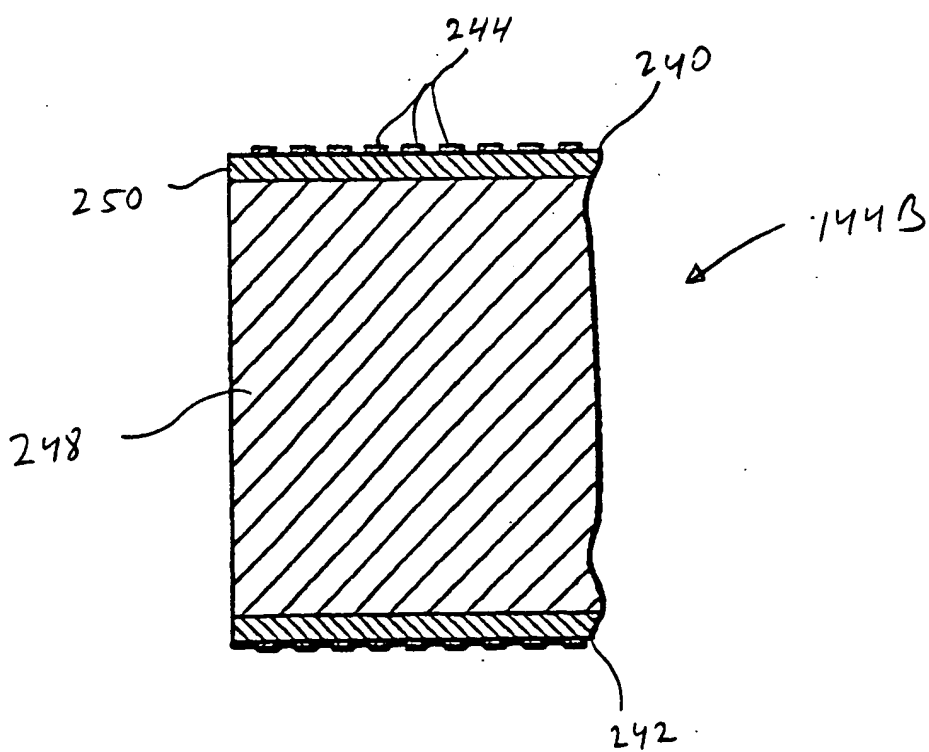


FIG. 13

FIG. 15

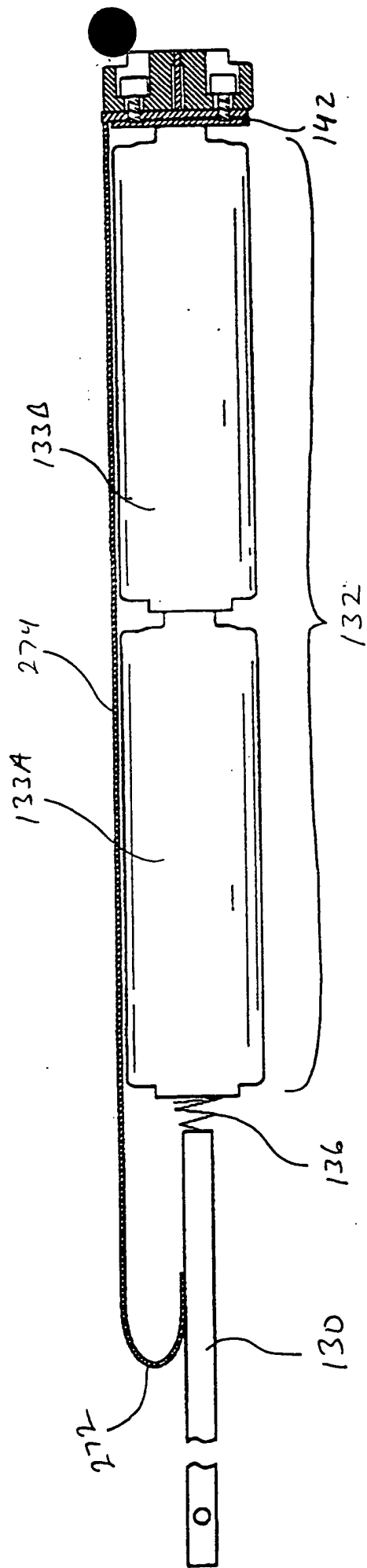


FIG.16

```

graph TD
    Start([Power On]) --> Init[Initialize]
    Init --> Loop(( ))
    Loop --> Command{Command in Queue?}
    Command -- Yes --> Execute[Execute Command]
    Execute --> Loop
    Command -- No --> Schedule[Schedule Clock Interrupt]
    Schedule --> Sleep{{Sleep}}
    Sleep -- Communications Interrupt --> HandleComm[Handle Communications Interrupt]
    HandleComm --> Loop
    Sleep -- Clock Interrupt --> HandleClock[Handle Clock Interrupt]
    HandleClock --> Loop

```

FIG. 17

```

graph TD
    A([Start Test Cmd]) --> B1[Begin Test.  
Turn on Circuits.  
Program Interrupts.]
    B1 --> A1([Idle])
    
    B([Measurement Interrupt]) --> B2[Perform Measurement.  
Submit Log Data Command.]
    B2 --> B1
    
    C([Log Data Command]) --> C1[Log Data.  
Adjust Sample Schedules.  
Program Interrupts if needed.]
    C1 --> C1
    
    D([End Test Cmd]) --> D1[End Test.  
Turn off Circuits.  
Turn off Interrupts.]
    D1 --> D2([Idle])
    
    A1 --- Repeat[Repeat as needed]
    B1 --- Repeat
    C1 --- Repeat
    D2 --- Repeat
  
```

The flowchart illustrates the test sequence with four main stages, each represented by a vertical column of boxes and ovals. Stage A starts with 'Start Test Cmd' (oval) leading to 'Begin Test. Turn on Circuits. Program Interrupts.' (rectangle), which leads to an 'Idle' (oval) state. Stage B starts with 'Measurement Interrupt' (oval) leading to 'Perform Measurement. Submit Log Data Command.' (rectangle), which loops back to the 'Idle' state. Stage C starts with 'Log Data Command' (oval) leading to 'Log Data. Adjust Sample Schedules. Program Interrupts if needed.' (rectangle), which leads to an 'Idle' state. Stage D starts with 'End Test Cmd' (oval) leading to 'End Test. Turn off Circuits. Turn off Interrupts.' (rectangle), which leads to an 'Idle' state. A bracket at the bottom connects the 'Idle' states of all four stages, labeled 'Repeat as needed'.

FIG. 18

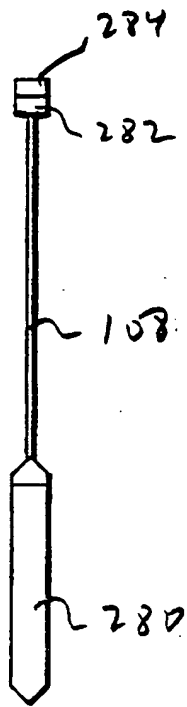


FIG. 19

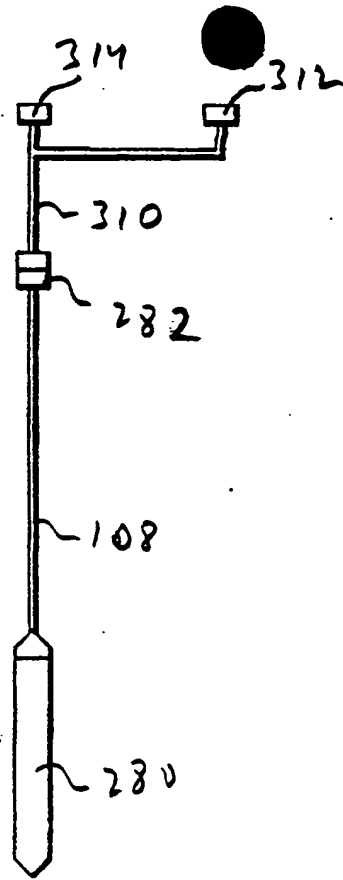


FIG. 24

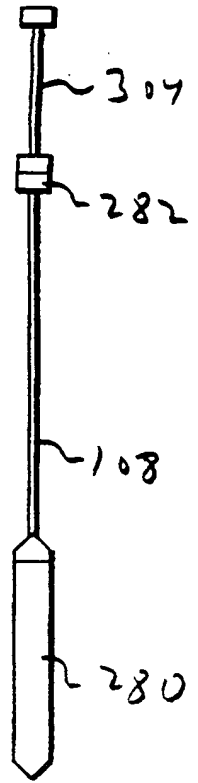


FIG. 23

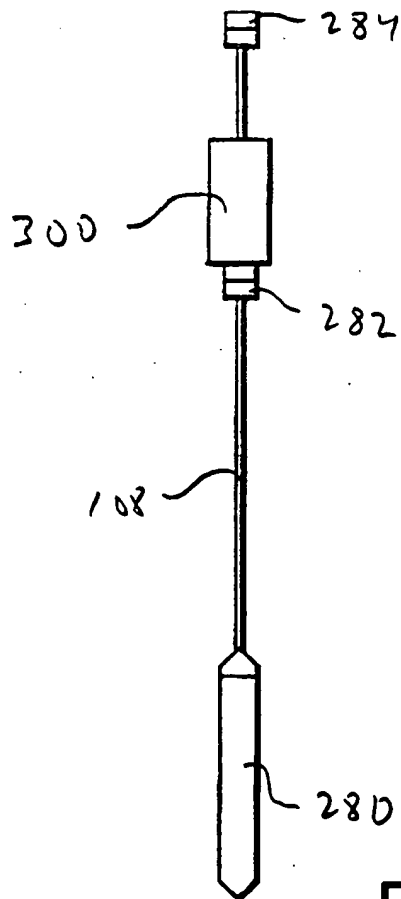


FIG. 22

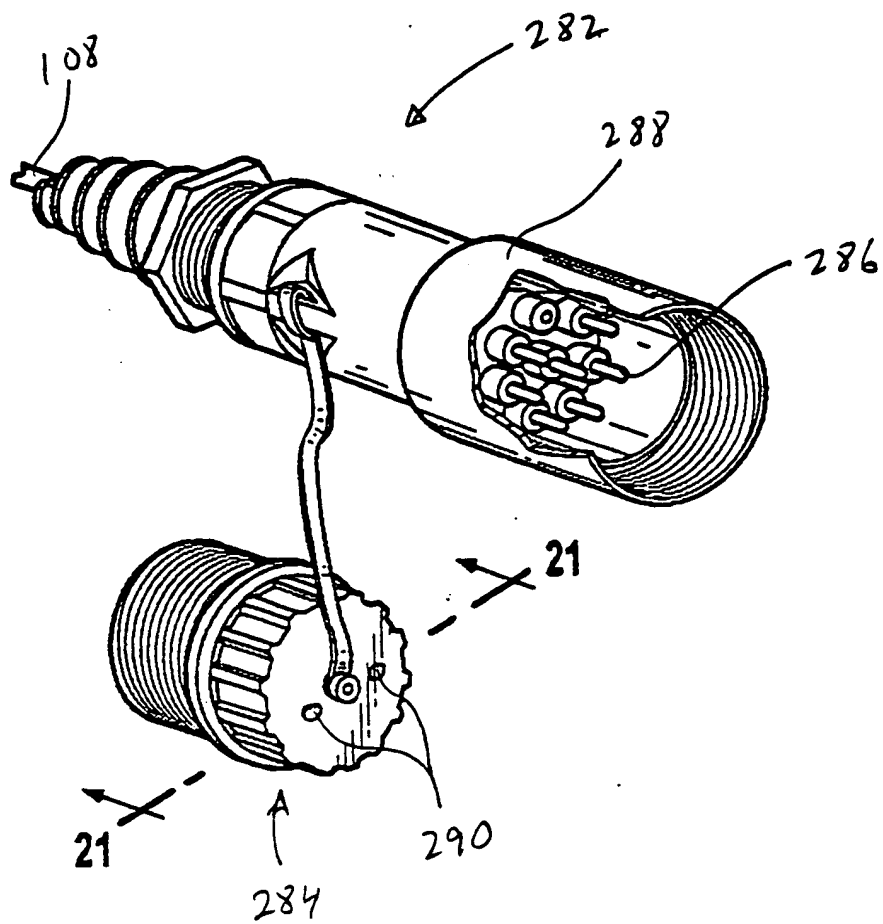


FIG.20

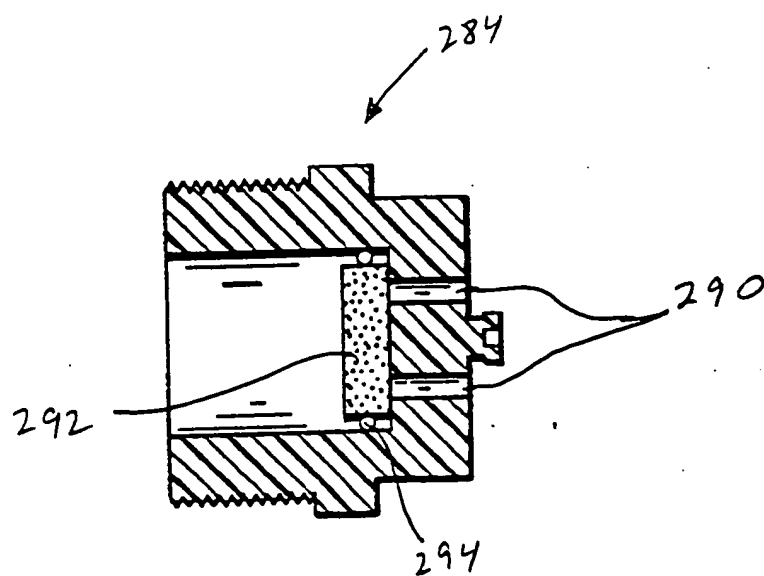


FIG.21

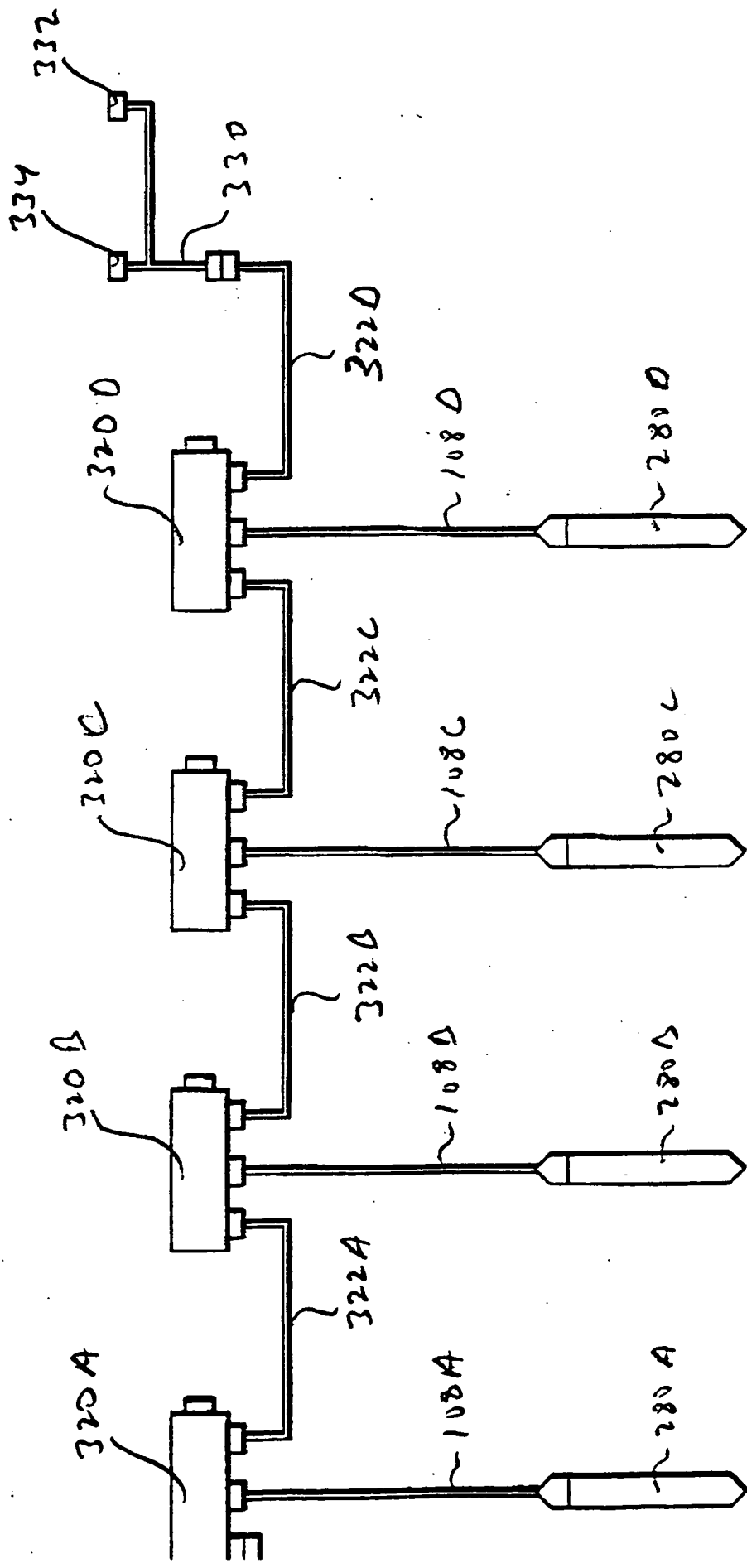


FIG. 26

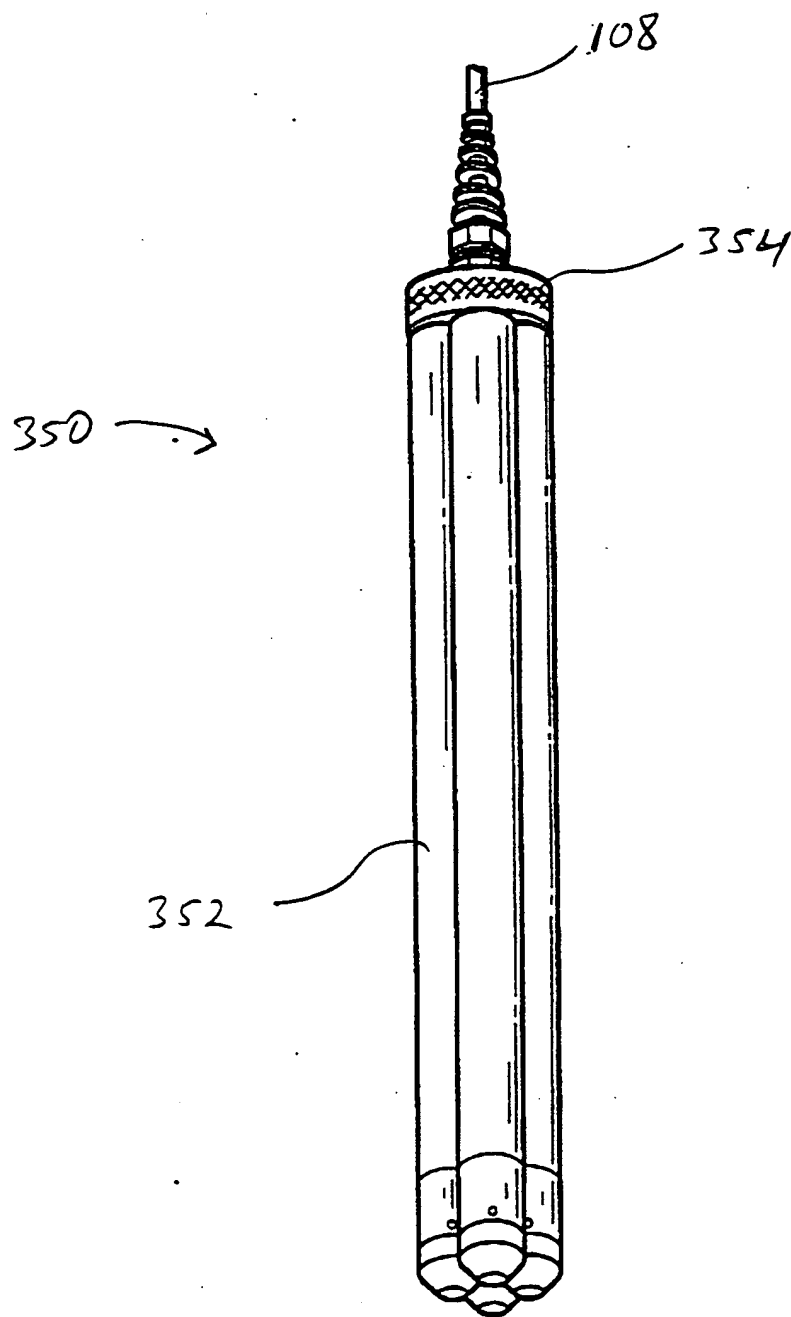
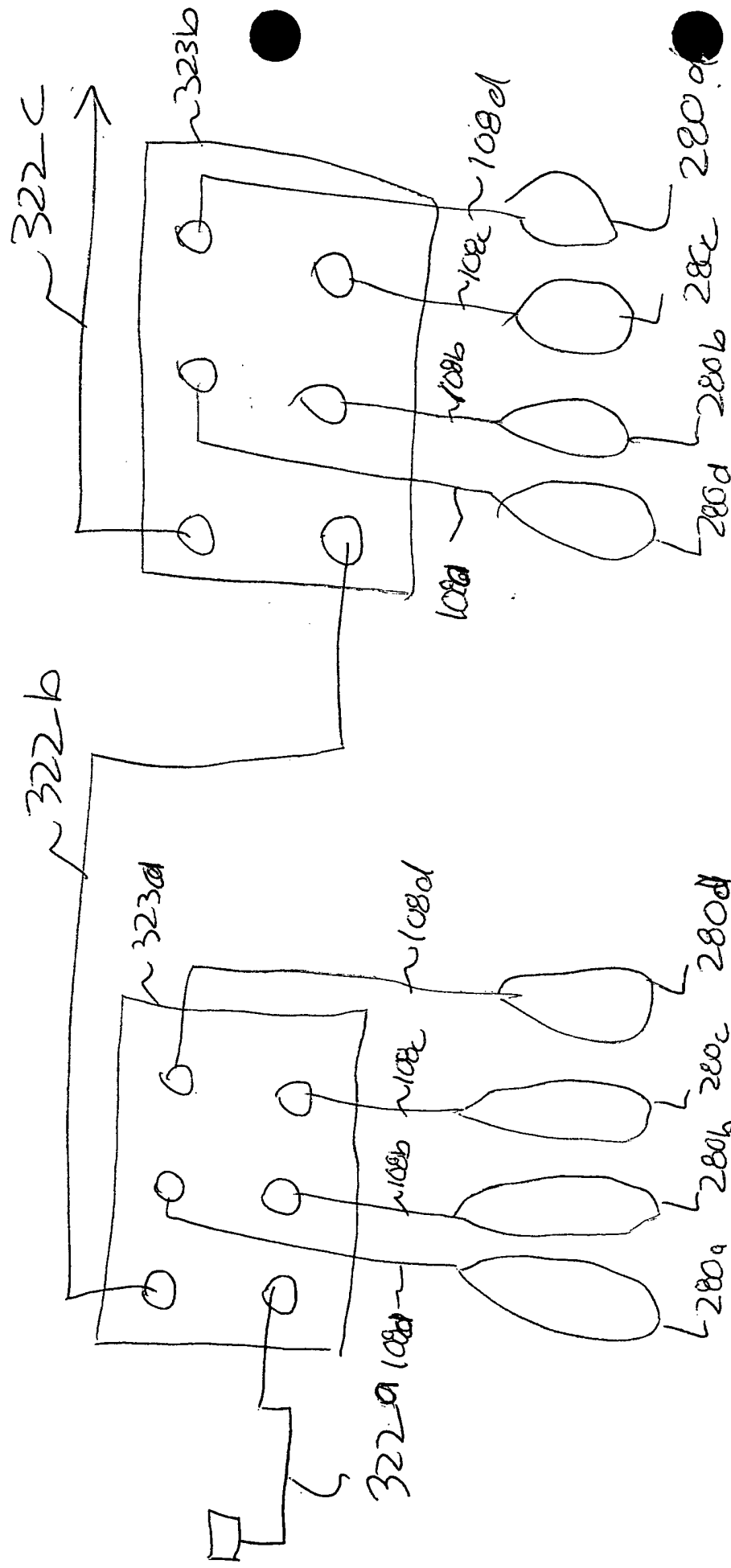


FIG.27

[illegible]

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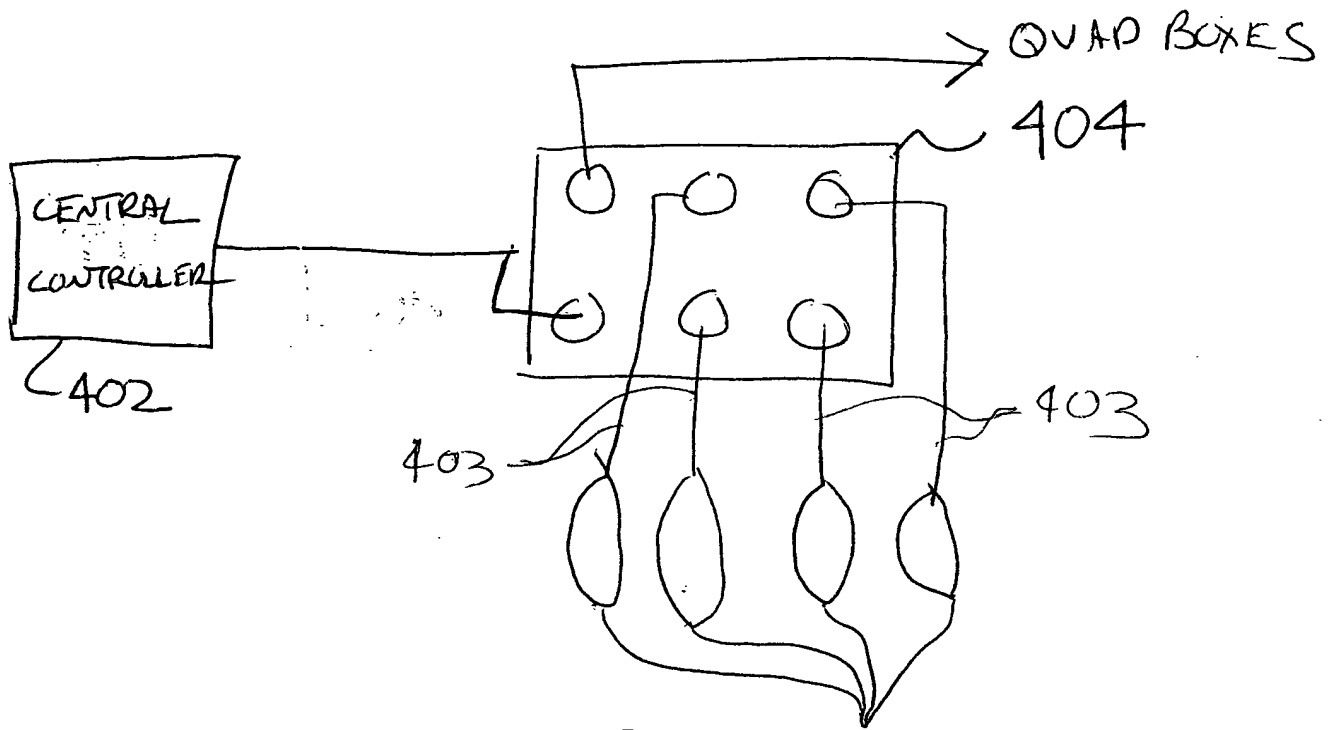


FIG. 29 a 406

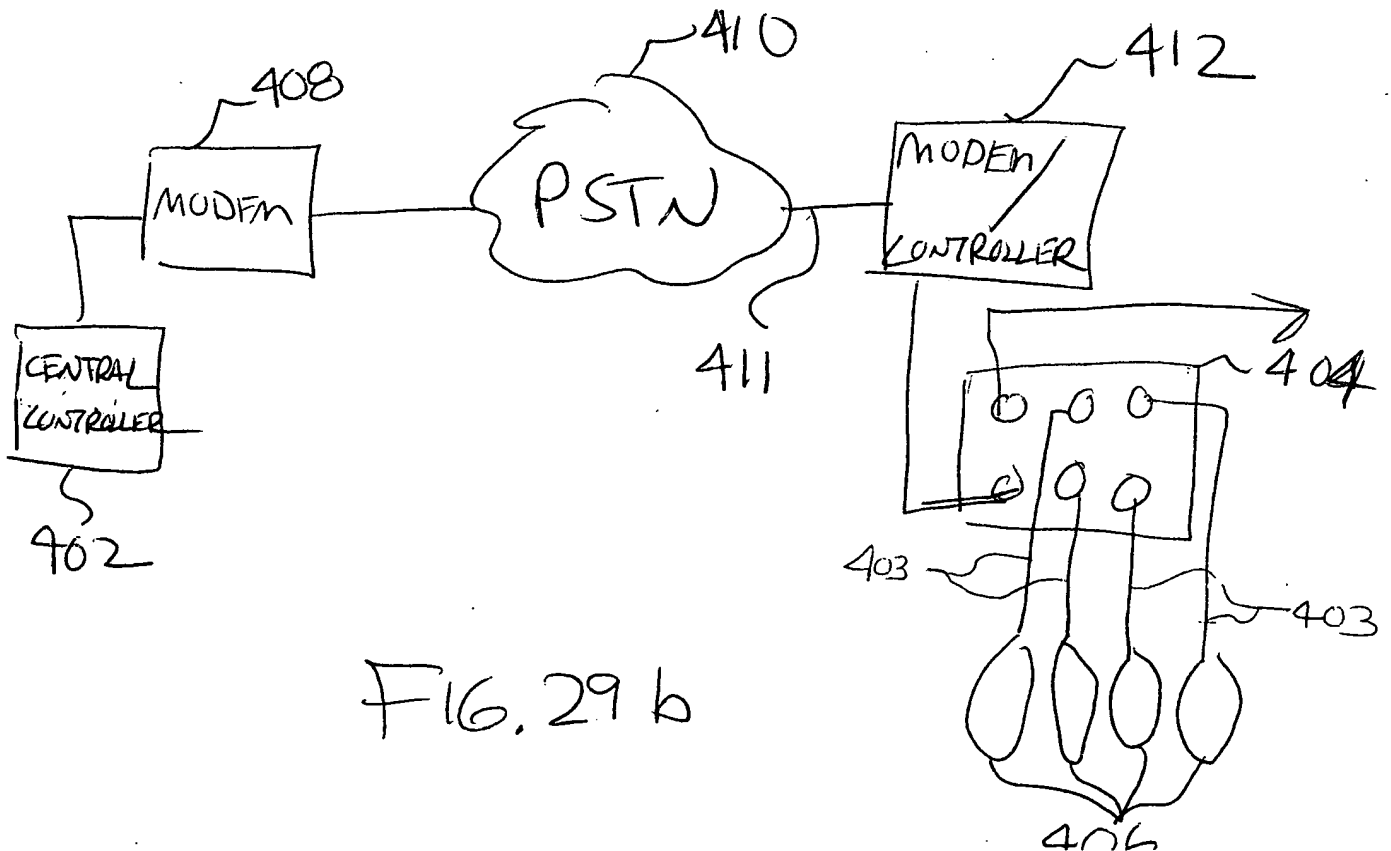


FIG. 29 b

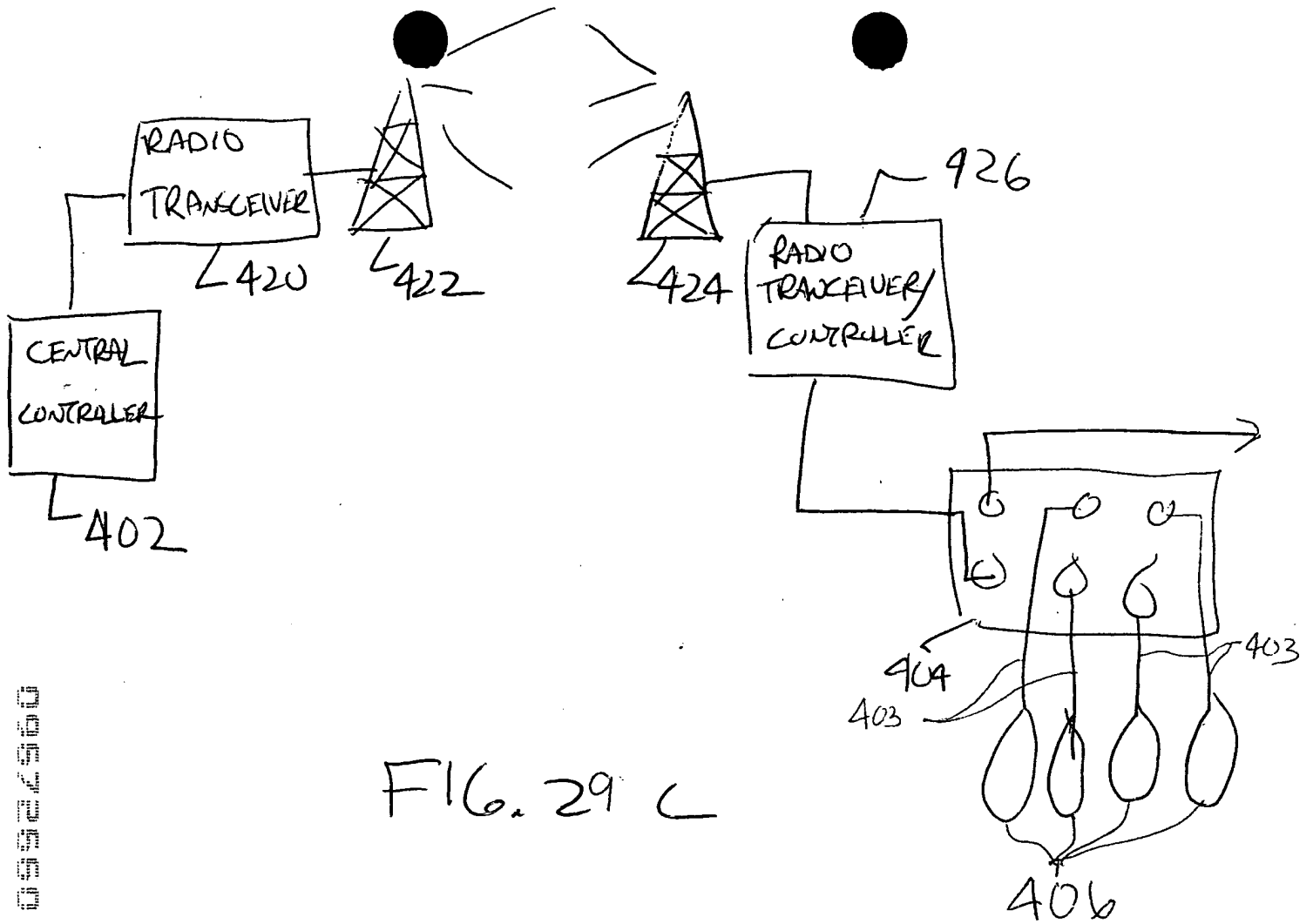


FIG. 29c

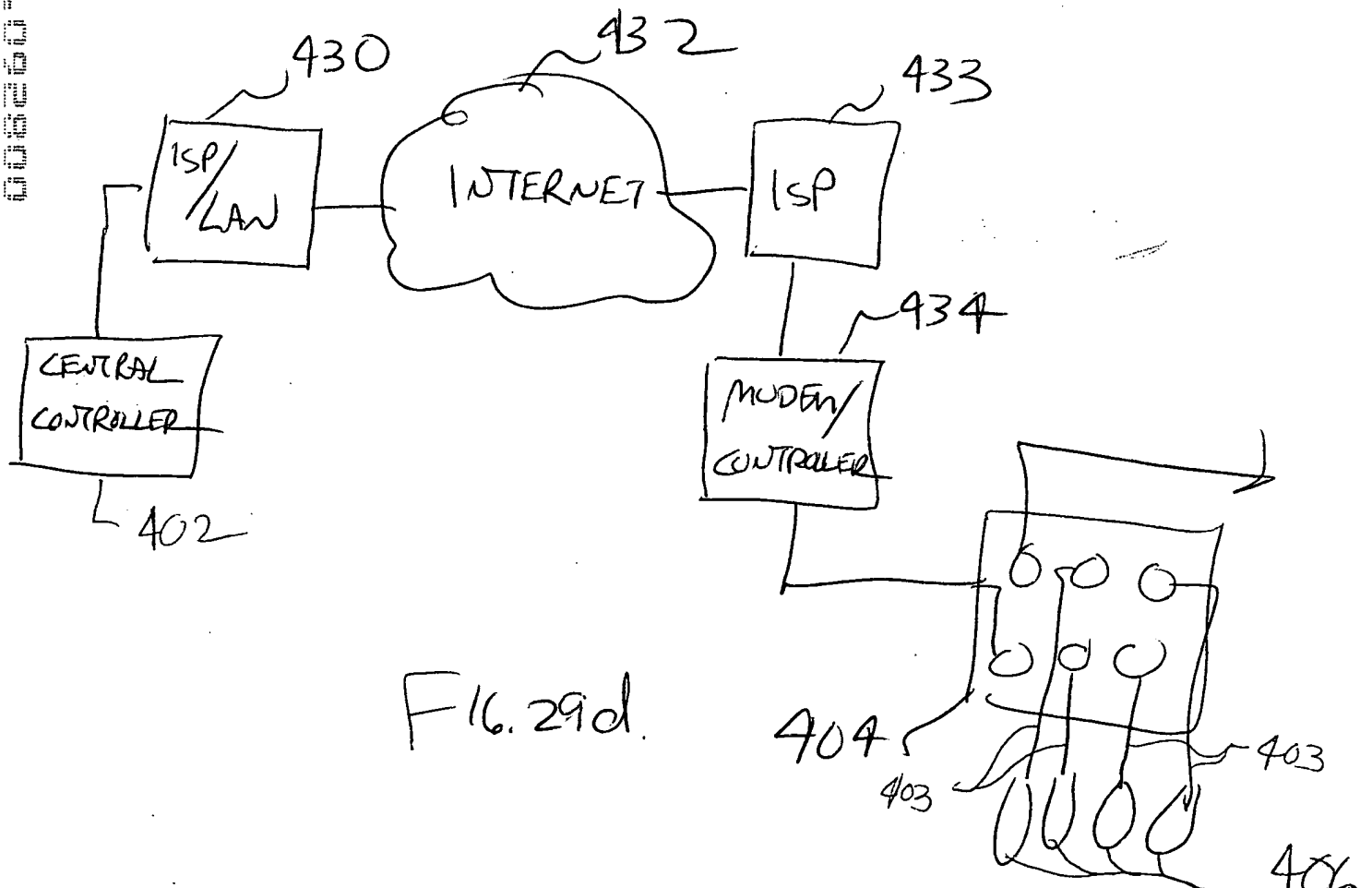


FIG. 29d

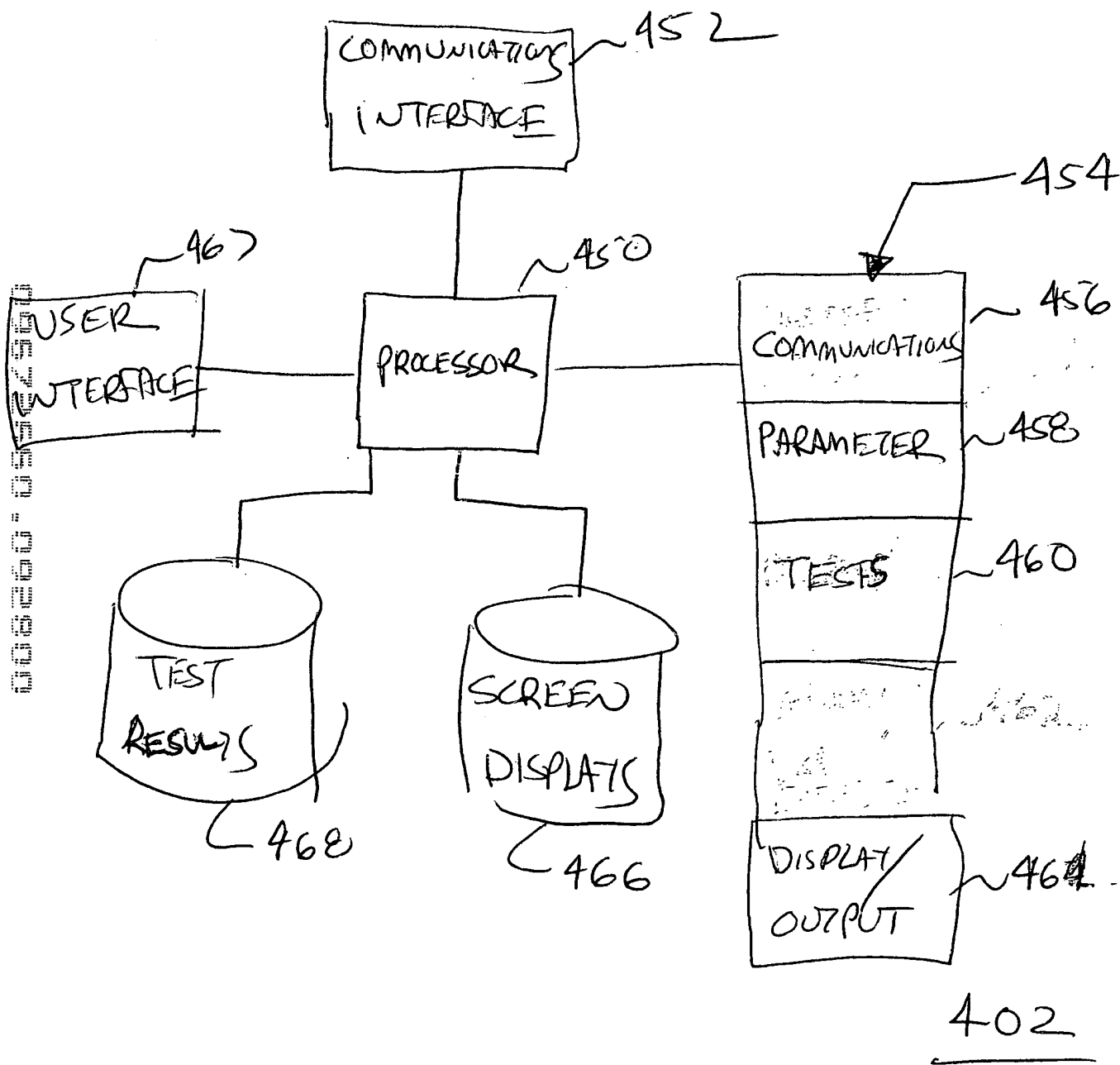


FIG 30

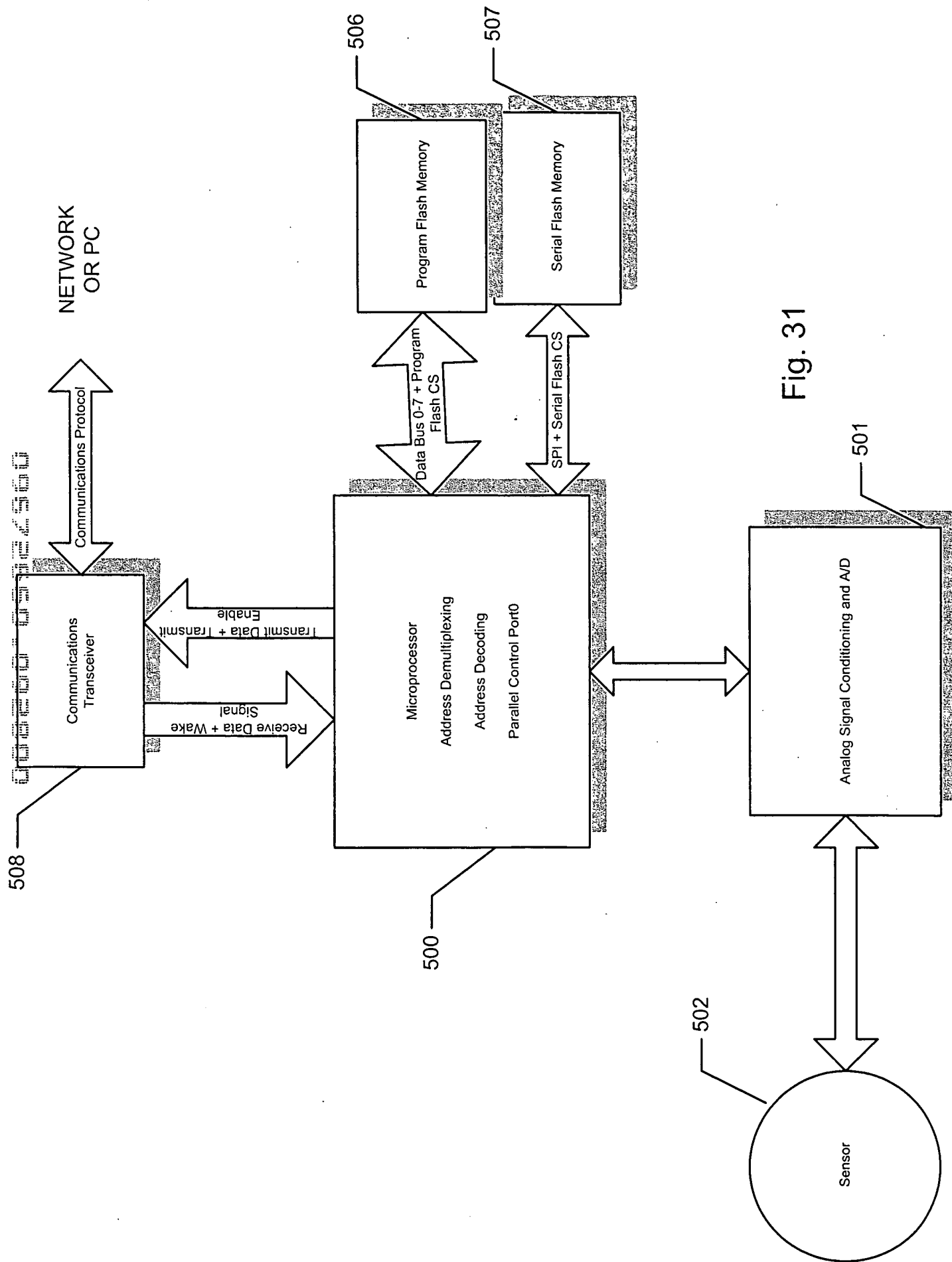


Fig. 31

```

graph TD
    A[GENERATE MESSAGE WHICH INCLUDES GENERAL ADDRESS HEADING] --> B[TRANSMIT MESSAGE OVER NETWORK]
    B --> C[MONITOR FOR RETURN MESSAGES]
    C --> D{MESSAGE RECEIVED ?}
    D -- YES --> E[ADD TOOL ASSEMBLY TO DIRECTORY FOR COM PORT]
    E --> F[PREPARE NEW MESSAGE EXCLUDING DEVICES WHICH HAVE RESPONDED]
    F --> A
    D -- NO --> G{TIME PERIOD EXPIRED ?}
    G -- YES --> H{RETRY COUNT EXPIRED ?}
    H -- YES --> I([END])
    H -- NO --> B
    G -- NO --> B

```

FIG. 32

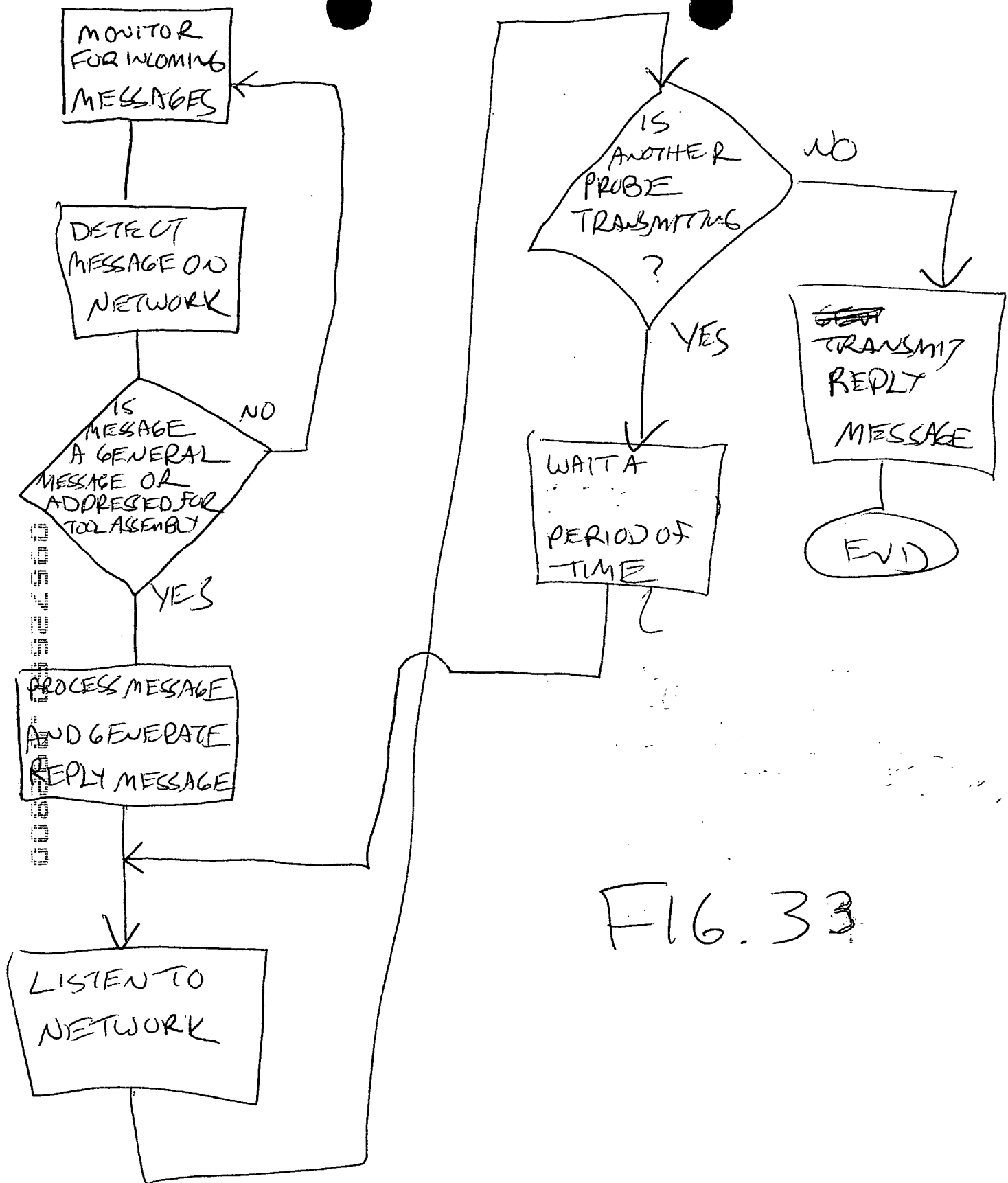


FIG. 33

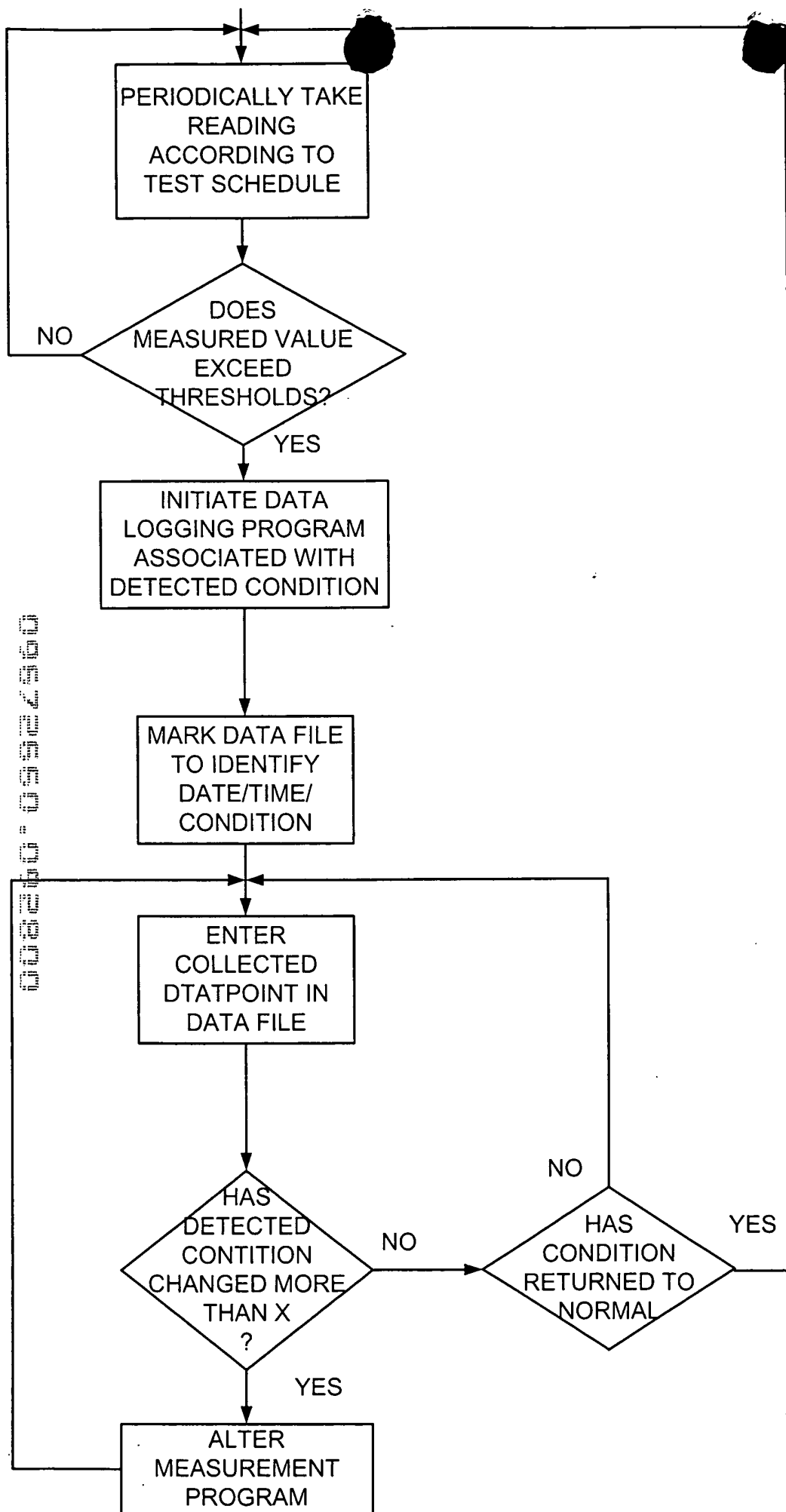


FIG. 34

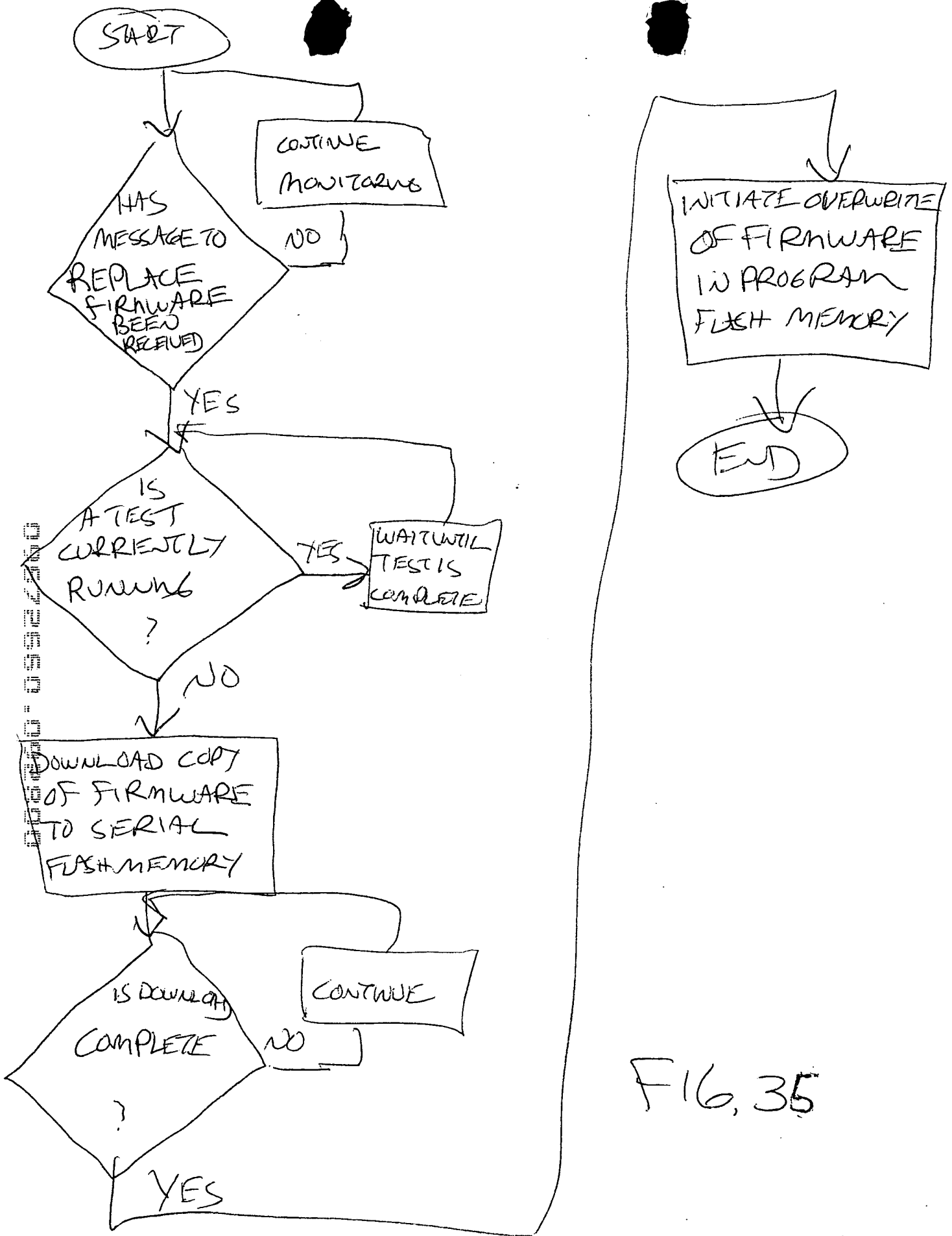


FIG. 35